Full Adder

Lab 2 ENEE 245

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**Objective**:

Digital logic anaylsis accomplishes many unique products and sums for circuit performance. Specificlly, full adders are diagnosed throught the entire lab by testing data after building a basic full adder on breadboards. Rise time, fall time, and propagation delay are studied on the oscilloscope to fully comprehend full adders.

**Design**:

The full adder is requiring only NAND and XOR gates for constructing the design and implementing onto the breadboard.

Truth Table 1:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Intput |  | Output |  |
| A | B | Cin | Sum | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Diagram

Description automatically generatedThe theoretical side of full adders consists of binary addition with three inputs. Two outputs returns the sum and cout/carry in again in binary. From the truth table, a K-map for both sum and cout/carry derives a sum of product equation. In general groups must contain 2^n cells to obtain elements, after grouping equations easily accessed. Initially, Sum: A’B’C + A’BC’ + AB’C’ + ABC, and Cout: AB + AC + BC. Final simplicfication for SOP of Sum: Cin ⊕ (A ⊕ B) and SOP of Cout: ((A ⊕ B)Cin) + (AB). Once fully simplified the logic diagram is deployed as follows:

Figure 1: Completed full adder logic diagram for Sum and Cout. Notice, a horizontal line through the diagrams center produces two logic. One for Sum and the other for Cout.

**Hardware**:

* Oscilloscope
* One 7486 Quad Exclusive-Or
* Two 7400 Quad 2-input NAND
* Breadboard
* Jumper Wire kit
* Two set of alligator clips
* Power Supply
* One D15-D0 probe

**Experiment**:

Graphical user interface

Description automatically generated

Figure 2: Displays X, Y, Cin, Cout corresponding to square graph. Square graphs gives one or zero as the output.

The 74163 synchronous 4- bit counter allows binary counting. For the purpose of a full adder, counter estaially count input data to return total sum and cout. Numbers are essential parameter for life, this counter helps builds calculator, timers, and full adders. Like any other chip, once powered the 74163 measures and displays binary numbers; one’s and zeros. In figure 2, along the x-axis is time at output. Following horizontal line through the square wave obtains a 4-bit binary number.

Diagram, schematic

Description automatically generated

Figure 3: Displays a connection diagram of 74163

The chip pins connected to as follows:

1. Clear is connected to the voltage source because activating clear will skew data. For casual operations like measuring chips voltage does not need clear varying inputs.
2. Clock is connected to the TTL output which is from the funciton generator.

3 - 6 pins are input notches not used.

7. Enable P is turn on by connnecting to postive notch. P is one of the gears that help function the 74163 chip

8. To prevent voltage overload there is ground set to a negative postion on the breadboard

9. Load is on by a positive notch with the voltage source

10. Enable T is turn on the positive voltage side

11 – 14 are output evaluated by the D15-D0

15. Is not used

16. Vcc is obviously connected to positive

Outputs of Qa, Qb, Qc, and Qd are in figure 2. There are two combinations of X, Y, Cin making them not slightly unique. Once I connected all outputs on the ocilloscope, each notch was disconnected individually the missing square wave was then identified.

Graphical user interface

Description automatically generated

Figure 4: Each square wave is labed Cout, X, Y, Cin

A picture containing text, electronics, display

Description automatically generatedCompeting the circuit was interesting. Figure 2 distinguished all output from 74163, from the original labels a complete circuit can be developed. QA/Cin, QB/Y, QC/X, QD nodes connected to a NAND chip and a Exclusive or chip. After careful wire manipulation a full bit adder circuit was connected to the counter chip. The initial fuller adder square waves for Cout displayed incorrect numbers. The circuit needed a minor change to create correct values.

Figure 5: Displays the rise time on the oscilloscope

A picture containing text

Description automatically generatedA picture containing text, electronics, display, computer

Description automatically generated

Figure 6: Displays propigation delay between sum and cout

The rise time of sum 3.2ns and the fall time is 3.4ns. The rise and fall are very similar in time. Rise and fall time were measured in similar fashion. Sum’s square wave beginning edge and end are horizontally zoomed into the screen. Run/Stop freezes to a frame to easy viewing, and single switched to different ranges a specific scale.

Figure 5: The fully complete full adder on a breadboard

**Analysis**:

The full adder circuit correcly adds and carries binary digits to output. With time and patience the circuit was made in time. To figure 4, verifying specifc data is quite simple. Input X: 0 Y: 1 Cin: 0 produces Sum: 1 and Cout: 0. This proced can be used through the whole data set and can confirm yourself the data is correct. Other then circuit misplacement for full adders initial display there were not much complications. I had to refresh my full adder truth table to be able to create the logic diagram.

**Conclusion**:

A full adder was developed on a breadboard for anaylsis of synchronous counters and ENEE 244 topic 1 bit adders. Hooking the counter up to the oscilloscope to determine logical placement of X, Y, Cin, Sum, Cout define the whole circuits trajectory. After confirm specific sections X, Y, Cin were used to create a full add with chips of NAND and Exclusive-or. The final product is a truth table on the oscilloscope and can also produce sum.

**Appendix**:

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